THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 40

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TOYOHIKO YOSHIDA

Appeal No. 96-2237
Application 08/113,509[1]

ON BRIEF[2]

Before THOMAS, KRASS and RUGGIERO, Administrative Patent Judges.

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[1] Application for patent filed August 27, 1993. According to appellant, the application is a continuation of Application 07/547,886, filed July 2, 1990, abandoned.

[2] Appellant's attendance at the oral hearing set for May 3, 1999 was waived in a fax communication received on April 23, 1999.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellant has appealed to the Board from the examiner's final rejection of claims 14 through 26, which constitute all the claims remaining in the application.

Representative claim 20 is reproduced below:

20. In a data processing system having a processor, a data memory, an instruction memory, an address bus, a data bus, an instruction bus, and a control bus, a method for accessing said data memory and said instruction memory, said method comprising the steps of:

placing on said address bus a first address which is either an instruction address or a data address, and placing on said control bus a first value indicating whether said first address is an instruction address or a data address;

latching said first address in either said instruction memory or said data memory, as designated by said first value;

ceasing to place said first address on said address bus and ceasing to place said first value on said control bus;

placing on said address bus a second address which is the other of an instruction address and a data address, and placing on said control bus a second value indicating whether said second address is an instruction address or a data address;

latching said second address in the other of said instruction memory and said data memory, as designated by said second value;

ceasing to place said second address on said address bus and ceasing to place said second value on said control bus;

placing first memory contents, addressed by either said first or second address, on the corresponding one of said data and instruction busses;

placing second memory contents, addressed by the other of said first and second addresses, on the corresponding other of said data and instruction busses,

wherein said first address is either an address for a single instruction word or an address for a single data word.

The following reference is relied on by the examiner:

Johnson et al. (Johnson) 4,851,990 July 25, 1989 (filed Feb. 9, 1987)

Claims 14 through 26 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Johnson alone.

Rather than repeat the positions of the appellant and the examiner, reference is made to the briefs and the answer for the respective details thereof.

OPINION

We sustain the outstanding rejection of claim 20 only and reverse the rejection of claims 14 through 19 and 21 through 26.

Johnson operates his RISC processor system utilizing a shared address bus in a manner to accommodate both pipelined and burst modes of operation where, in the burst mode, simultaneous

or concurrent transfers of data and instructions over independent data and instruction busses occurs. In pipelined instruction and data accesses, the pipelined or second instruction access cannot complete until the first access has been completed. Addition- ally, only instruction accesses may be pipelined or only data accesses may be pipelined but not either in a sequential order. Note column 6, lines 8 through 14, and column 7, lines 9 through 14. Therefore, the pipelined teachings of Johnson may not be used by the examiner to reject independent claims 14 and 21 on appeal which require that the first and second access cycles be either a data

access followed by an instruction access or vice versa. See also the teachings at column 11, lines 13 through 25.

On the other hand, the burst-mode access, which is discussed beginning at column 12, line 45, permits such alternative or overlapped accessing between data and instruction accesses. The examiner's arguments at page 3 of the answer are aptly characterized by appellant at page 11 of the brief as an attempt by the examiner to combine the pipelined and burst-mode protocols. We do not agree with appellant's view that Johnson teaches away from this combination but only that the two modes

are distinct and separate within the context of Johnson alone and well recognized in the art as distinguished anyway. The modified so-called simple access to include a later pipelined access or burst-mode access discussed at column 10, line 55, through column 11, line 2, also does not argue for combining the pipelined and burst-mode accesses in Johnson.

The examiner's reasoning at page 3 of the answer is presumptuous, and the mere fact that an existing data struc-

ture could be capable of supporting a certain functionality does not necessarily mean that it would have been obvious to do so absent some independent evidence or argument to the contrary. The mere fact that the examiner considers something obvious because nothing may prohibit it is not persuasive within 35 U.S.C. § 103 that some functionality would have been obvious to the artisan. There is nothing within Johnson and there is no persuasive approach argued by the examiner to us that leads us to believe that the artisan would have prospectively combined the teachings of both the pipelined and burst-mode protocols into one common functionality based upon Johnson's teachings alone and the knowledge of the artisan combined therewith.

As to independent claims 14 and 21, appellant argues at the bottom of page 11 and again at the bottom of page 17 that "[a]s to both the pipelined and burst-mode protocol processors, a second access completes only after the first access completes."

Our study of Johnson leads us to agree with this assessment which prohibits the affirmance of the rejection additionally because
the teachings and showings in Johnson clearly would not have been able to meet the requirement of the processor completing the second access cycle before the first access is complete, a feature common to both independent claims 14 and 21 on appeal.

Therefore, the rejection of independent claims 14 and 21 and their respective dependent claims must be reversed.

We reach an opposite conclusion, however, as to independent method claim 20 on appeal. To the extent recited in this claim, we note that certain input latches are noted to exist in the art although not shown in Johnson in the discussion beginning at column 5, line 55. Claim 20 recites that there is placed on the address bus a first address, it is latched in the respective memory and then the process ceases to activate the address on the address bus. This three step process is repeated in the claim for the "other" of the instruction address and data address. The claim then recites

placing the respective memory contents on either of the respective instruction or data busses. There is no requirement in claim 20, as in independent claims 14

and 21, that the processor complete the second access before the first access is complete. Appellant's just quoted view at the bottom on pages 11 and 17 of the principal brief on appeal apparently confirms our assessment on the operation of Johnson.

We do not agree with appellant's view expressed at page 14 as to claim 20 that Johnson teaches asserting the address of the first access on the address bus until the address memory contents appear on the corresponding instruction or data bus in a manner contrary to the recitations in claim 20. There is no such recitation in claim 20. Appellant's views go on to indicate that only after the address memory contents appear on the bus does the burst-mode protocol cease to assert the address of the first access and allow the assertion of the address for a second access, by making reference to Figure 6. Column 12, lines 45 through 47, of Johnson

state that a "burst-mode access allows multiple instructions or data words at sequential addresses to be accessed with a single address transfer." The argument is not coextensive with the teaching in the reference and the showing in Figure 6. The first appearance of INSTR N on the instruction bus line in this figure does occur before the end of the address existing on the corresponding address line, however, the access is not complete until all of the retrieved instructions have been

"accessed" by the processor. It is thus apparent that the address does end on the address bus well before the entire access cycle for the instruction is completed. A corresponding data read operation in the burst-mode access would yield the same
result.

Nor are we persuaded otherwise by the language at the end of claim 20 which indicates that the first address is either an address for a single instruction word or an address for a single data word. Clearly, to the artisan, a single

address transfer or a single address request for a single instruction word or a single data word is what is implemented in Figure 6 and for a corresponding data access as well. Only a single address is sought from which other addresses may be sequentially indexed in some manner as shown in Figure 6. Therefore, as to the ceasing operations recited, it is thus apparent that the address for the instruction in Figure 6 is ceased before accessibility begins for a corresponding data access operation and vice versa. Appellant's arguments in the reply brief as to claim 20 do not persuade us otherwise.

In view of the foregoing, the decision of the examiner rejecting claims 14 through 26 under 35 U.S.C. § 103 is affirmed

only as to claim 20. Therefore, the decision of the examiner is affirmed-in-part.

No time period for taking any subsequent action in con- nection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

JAMES D. THOMAS Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH RUGGIERO Administrative Patent Judge	)	

JDT:psb

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